

**Department of Physics**

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| Course Number | COE328 |
| Course Title | Digital Systems |
| Semester/Year | Fall 2021 |
| Instructor | Dr. Reza Sedaghat |
| TA Name | Sajjad Rostami Sani |

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| Lab Report No. | 1 |
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| Report Title | Lab 1 |

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| Section No. | 03 |
| Submission Date | 27-Sept-2021 |
| Due Date | 27-Sep-2021 |

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| Student Name | Student ID | Signature\* |
| Ahmad El-Gohary | 501011852 |  |

\*By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at:

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**Objective**

The objective of this lab was to get familiar with designing digital circuits in Quartus 2 and learn how to code a block function.

**Procedure**

Part 1

* Diagram

  Description automatically generatedBuild the circuit in the following schematic using input pins for x1,x2,x3 and an output pin to f.
* Compile the circuit (Ctrl+L)
* A picture containing text

  Description automatically generatedAssign the pins the following values using assignment editor (ctrl+shift+A) to open pin assigner



* Click on add a new pin from and click on the logo next to the drop-down arrow
* Add all pins to the table from this windowGraphical user interface, application

  Description automatically generated
* Recompile the circuit to assign the pins

To get the time graph of the circuit

* File > New > Verification/Debugging Files > University Program VWF to open the graph editor
* Add all pins and add all the values for only the input pins Chart

  Description automatically generated
* Compile the graph to get the out put function

A picture containing calendar

Description automatically generated

Part 2

* Open a new file Select File -> New, choose VHDL File
* Graphical user interface, text, application, email

  Description automatically generatedWrite this 1st code

Insert this line where it says –insert code here

(x1 \* x2) + (!x2 \* x3)

* Write this 2nd code Graphical user interface, text, application, email

  Description automatically generated

Insert this line where it says –insert code here

x1= w1\*w2+w3\*w4

x3=w1\*w3+w2\*w4

* Export the codes as block circuits “File -> Create/Update -> Create Symbol Files for Current File”
* Connect both circuits as follows

Diagram, schematic

Description automatically generated

* Compile the circuit (Ctrl+L)
* Assign the pins the following values using assignment editor (ctrl+shift+A) to open pin assigner



* Click on add a new pin from and click on the logo next to the drop-down arrow
* Add all pins to the table from this windowGraphical user interface, application

  Description automatically generated
* Recompile the circuit to assign the pins

To get the time graph of the circuit

* File > New > Verification/Debugging Files > University Program VWF to open the graph editor
* Add all pins and add all the values for only the input pins A picture containing chart

  Description automatically generated
* Compile the graph to get the out put function

A picture containing table

Description automatically generated

**References**

Brown, S. D., & Vranesic, Z. G. (2009). *Fundamentals of Digital Logic with VHDL Design*. New York, United States: McGraw-Hill Education.